

iMAPS 2018 HITEC



9:30AM May 8, 2018

Sixty Earth-Days Test of a Prototype Pt/HTCC Alumina Package in Simulated Venus Environment

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Background

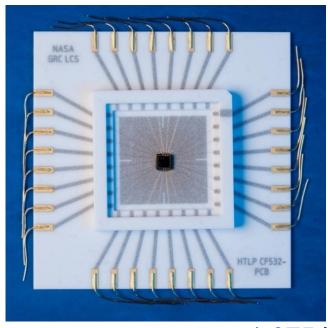
- 500 °C operable electronics for NASA aeronautics and space applications
- Packaged SiC JFETs based analog and digital ICs tested at 500 °C for over 10k hours, and briefly tested at T over 800 °C
- Packaging system with HTCC alumina and AuPt metallization developed and tested with SiC ICs
 - 32-I/O package and compatible PCB
 - 500 °C die-attach
 - Au alloy wire-bonds
- Durability in Venus environment?
 - 465 °C, 90 bar pressure and corrosive gas ambient
 - Previous Venus missions were all short-lived
- HTCC alumina substrate with Pt metallization supported a SiC ringoscillator test in simulated Venus environment for 3 weeks







Test Assembly of a SiC IC with HTCC Alumina Packaging System



1.075 in.

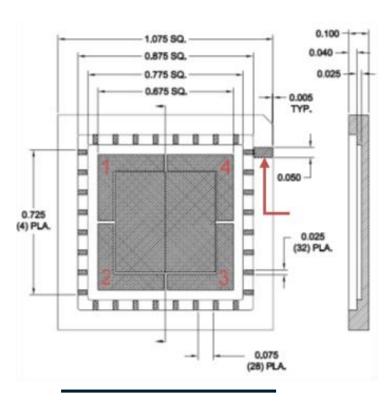
- Packaged SiC IC with Pt/HTCC alumina package and PCB
- PCB measures 2 inch x 2 inch, Pt traces co-fired with alumina
- 1 mil Au alloy wire thermo-sonically bonded



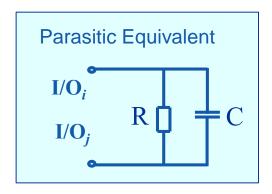




Parasitic R//C of Neighboring I/Os



1.07 inches



R//C model

R – DC leakage and AC dielectric loss

C – Dielectric polarization

$$1/Z(T,\omega) = G(T,\omega) + j\omega C(T,\omega)$$

R//C measured between I/O1 - I/O2, and 1/02 - 1/03

 I/O1 connected to all five bias pads DC resistance measured separately







AC Parasitic Capacitance and Conductance of Neighboring I/O1 - I/O2

f (Hz)	T_R	100	150	200	250	300	350	400	450	500	550	
120	1.0	0.7	0.6	0.4	0.3	0.5	0.4	0.6	0.7	1.4	1.4	
	< 0.001	< 0.001	< 0.001	< 0.001	< 0.001	< 0.001	< 0.001	< 0.001	< 0.001	0.001	< 0.001	> 50°C margin
1K	0.4	0.2	0.5	0.5	0.3	0.4	0.5	0.5	0.5	0.5	0.4	above 500°C
	< 0.001	< 0.001	< 0.001	< 0.001	< 0.001	< 0.001	< 0.001	< 0.001	< 0.001	< 0.001	< 0.001	
10K	0.5	0.4	0.5	0.5	0.4	0.4	0.4	0.5	0.5	0.4	0.4	
	< 0.001	0.0013	< 0.001	< 0.001	< 0.001	< 0.001	< 0.001	0.003	< 0.003	< 0.003	< 0.003	
100K	0.5	0.3	0.5	0.4	0.3	0.4	0.4	0.5	0.5	0.4	0.4	
	0.01	0.016	0.014	0.016	0.016	0.011	0.014	0.029	0.035	0.026	0.045	pF
1M	0.5	0.4	0.5	0.4	0.3	0.4	0.4	0.5	0.5	0.4	0.5	μS
	< 0.010	< 0.010	0.013	0.012	0.011	0.006	0.009	0.018	0.021	0.022	0.026	

 $C < 1.5 pF, R > 20 M\Omega$

Usable for many envisioned 500°C SiC ICs

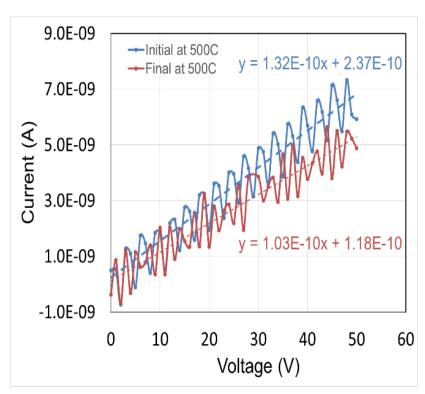


L. Chen, et al., Proc. IMAPS High Temperature Electronics Conference, 2016, pp. 66-72





DC Resistance of Neighboring I/Os



DC I - V Curves

- I-V curve between I/O27 and I/O28
- 500°C
- Wide DC bias range: 0 50V
- SMU: integration time 16.67 msec, time delay 0.1 sec
- I/O28 not connected to SiC die, I/O27 connected to isolated two-terminal test structure on SiC die
- Package mounted on PCB
- Slope of linear fits: $7.6 \text{ G}\Omega$ initially 9.7GΩ after 69.4 hrs
- DC resistance slightly underestimate
- Noise from running oven



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Experimental – HTCC Package

HTCC Alumina Package for Venus Ambient Test

Customer HTCC alumina package

- 1 in. x 1 in. x 0.1 in. HTCC package diced
- Two end parts jointed (the central par removed) with glass adhesive
- Reinforced using glass and ceramic adhesive
- Two packages tested
 - Pt pads of one package coated with thin film Au, Package 5
 - Pt pads of other package coated with thick-film Au, Package 4
- 8 x10 mil diameter Au wires attached
- A SiC IC attached using Au paste
- Two un-connected I/O (Wire 4 and 5) used for DC leakage monitoring

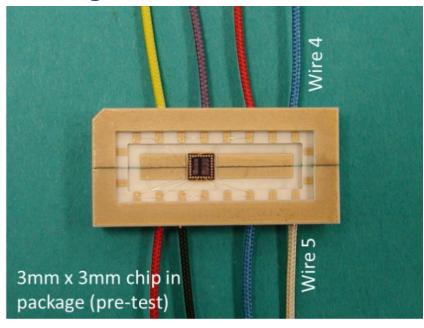






Experimental – HTCC Package

HTCC Package 5 for Venus Environment Test



- Package 5 for Venus environment test, a SiC IC attached and wire-bonded
- Two pads connected to Wire 4 and 5 for insulation test in simulated Venus environment
- A thin Au layer was coated on co-fired Pt metallization surfaces
- 1.075 in. x 0.5 in. x 0.1 in.
- The color coded glass fiber sleeves were baked before integration





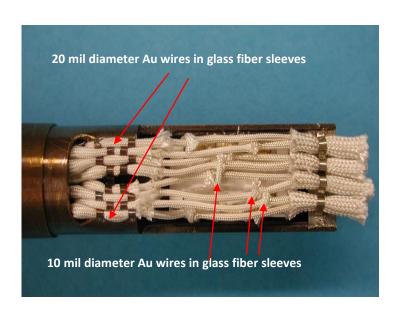


Experimental – Test Assembly

Test Assembly Integration

- Packaged SiC IC and leakage measuring pads connected to instrument via a feedthrough
- Eight Au wires on the package attached to eight 20 mil diameter Au wires
 - Low DC voltage sparkwelded
- Insulated with fiberglass sleeves
- No lid device and package fully exposed
- Stainless steel tube with a cap, the cap has an open end
- 20 mil diameter Au wires extend to a customer feedthrough





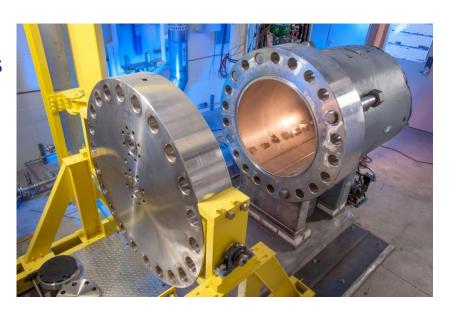




Experimental – GEER

NASA Glenn Extreme Environment Rig (GEER)

- The GEER chamber: 3 ft diameter and 4 ft long stainless steel pressure vessel
- With a fully automated high pressure gas delivery system
- Multi-gas mixer, and high pressure gas pump
- Uniformly heated by internal electric heaters



- Controlled by the facility programmable logic controller (PLC)
- This test in GEER included two test phases (Phase 2 and 3)
- A brief test in Earth air first







Experimental – Simulated Venus Environment

Simulated Venus Environment in GEER

- Purged with dry nitrogen gas and evacuated to 0.1 bar
- Filled pure nitrogen to 36.5 bar, the heated at 7 °C/hour to the target conditions of 460°C and 92 bar pressure
- Held for 48 hours, then reduced to 150°C and then depressurized to 1 bar
- Filled Venus simulating gas mix automatically at 150°C
- Heated at 7 °C/hr reaching 92 bar at 460 ± 5 °C
- Simulated Venus environment for 60 Earth days

Gas	Mixing (Mole) Ratio
CO_2	0.965
N_2	0.035
SO_2	18.0×10^{-5}
OCS	5.10 x 10 ⁻⁵
H_2O	3.00×10^{-5}
CO	1.20 x 10 ⁻⁵
H_2S	0.20×10^{-5}
HC1	5.00×10^{-7}
HF	2.50×10^{-9}







Experimental – Insulation Resistance Measurement

Insulation Resistance Measurements

- Resistances between Wire 4 and 5 measured to evaluate the parasitic leakage
- Package and wiring system leakages in parallel
- I V curves between Wire 4 and 5 measured at the other (outside-GEER) ends
- SMU: integration time 16.67 ms, time delay 0.1 s
- Resistance calculated from the slope of best liner fit of I-V curve
- I-V curves were scanned between 0 to 50V (or current compliance point)
- Resistance include package leakage between Wire 4 and 5 in parallel with the insulation resistance between two 20 mil diameter Au wire
- First characterized in Earth air ambient from room temperature to 465 °C (Phase 1)
- Phase 2 in high pressure N₂ (GEER N₂)
- Phase 3 in simulated Venus surface environment in GEER
- Measured during both upward and downward temperature ramps

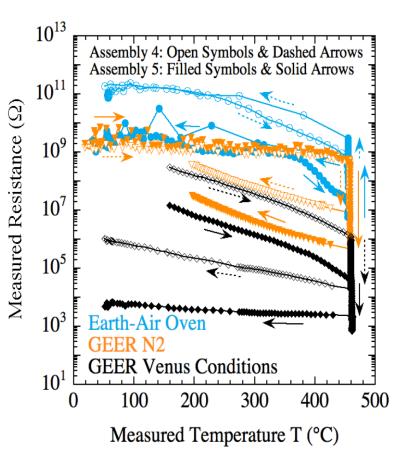






Results and Discussion – Electrical Insulation

Resistance vs Temperature – All three Phases



- Temperature dependent Wire 4 Wire 5 resistances of assembly 4 and 5
- Temperature ramps for Earth air, GEER N₂, and GEER Venus conditions, and constant temperature dwell at 460±5 °C
- Resistances decrease significantly with temperature, for all temperature ramps
- Temperature dependence of resistances approximately reversible in Earth air cycle
- Resistances changes in GEER N₂ and GEER Venus conditions not reversible
- The insulation resistances of both assemblies decrease severely and irreversibly in GEER N₂, Venus conditions
- Total drops of insulation resistances are over five orders of magnitude

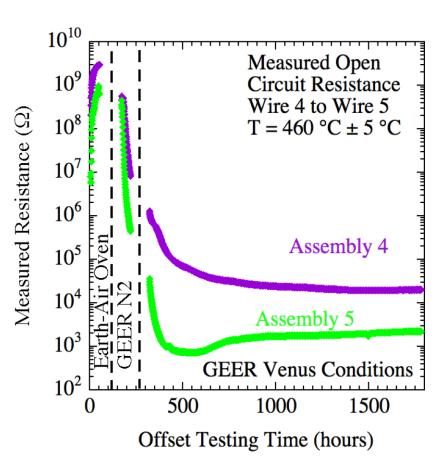






Results and Discussion – Electrical Insulation

Resistance vs Test Time at 460 °C – All three Phases



- · Earth air
 - Resistance of assembly 5 increases from 7.9 M Ω 650 M Ω
 - Assembly 4 resistance increases from 210 M Ω to 3.0 G Ω
- GEER N₂ at 90 bar
 - Assembly 5 resistance decreases from 384 M Ω to 448 k Ω
 - Assembly 4 resistance decreases from 424 $M\Omega$ to $7.6M\Omega$
- GEER Venus conditions
 - Assembly 5 resistance decreases from $45k\Omega$ to $2.26~k\Omega \sim 60~days$
 - Assembly 4 resistance declines from 1.18 M Ω to 19.8k Ω
- Insulation resistance degradation not reversible

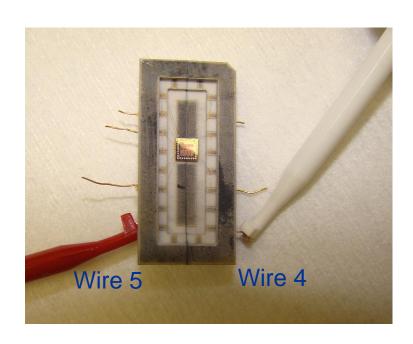






Results and Discussion – Post–Test Degradation Analysis

Post-Test Resistance Measurements



The electrical resistance between Wire 4 and Wire 5 was directly measured by clipping Au wires



Post-test analysis of Assembly 5

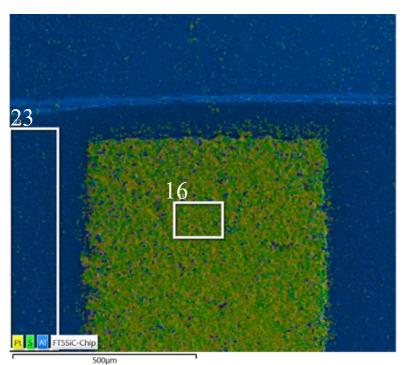
- I-V curves measured as being taken apart
- Prior to the disassembly, the roomtemperature insulation resistance between Wire 4 and Wire 5 was 12 kΩ
- Resistance between Wire 4 and Wire 5 was 21.7 MΩ, after disconnected from 20 mil Au wires
- Resistance between the corresponding long fiberglass-insulated 20 mil diameter Au wires was only 12 kΩ
- HTCC ceramic package excluded as the primary DC leakage source
- The insulation resistance between 5
 Wire 4 to 5 at room temperature
 substantially and permanently
 degraded to 21.7 MΩ





Results and Discussion – Surface Analysis

EDS Elemental Map of a Bond Pad



Pt







- Distributions of Pt, S, and Al indicated by yellow, green, and blue colors
- Box 16: weight percentage of Pt, Au, S, and Al measured are 47.1%, 36.4%, 9.4%, and 1.1% (other elements detected), respectively
- Cross section (not shown) study
 - Thin non-uniformed surface layer of PtS on bond pad
 - Underlying Pt is not reacted
- Box 23: weight percentage of Pt, S, C, and Al (O, Si, and Mg also detected) are 1.2%, 0.5%, 1.9%, and 53.4% (other elements detected), respectively

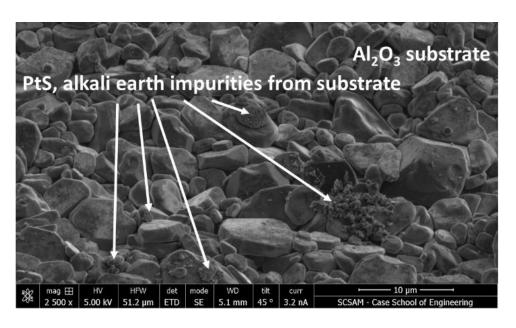






Results and Discussion – Surface Analysis

SEM/EDS and XPS Results of Alumina Surface Near Bond Pad



- FE-SEM micrograph of alumina surface ~ 45 µm x
 25 µm on the left side of the bond pad
- Scattered and isolated particles of PtS, and alkali earth impurities from the alumina detected
- EDS elemental map (not shown) of Au indicates Au distribution not uniform and continuous

- XPS of co-fired alumina surface
 - C, S, F, Na, Mg, Ca, Si, Fe, trace amounts of Pt, in addition to O and Al detected, C concentration is high
 - After 1 min. Ar+ sputtering, carbon significantly reduced, Ca eliminated

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Elements	С	Pt	Na	Mg	Ca	Fe	Si	S	F	0	Al
Prior sputtering	33.5	0	0.9	0.2	0.3	0.5	5.6	2.7	0.5	38.6	17.2
1 min. sputtering	7	0.2	0.3	0.3	0	0.9	1.9	1.2	0.3	57.9	30



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in Simulated Venus Environment

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Discussions and Summary

- Two customer HTCC alumina packages with Pt metallization tested in simulated Venus environment for 60 Earth days (with SiC IC)
- Bulk materials of co-fired Pt and 92% alumina chemically stable in 60 days of Venus environment
- Thin top layer of PtS observed on originally Au coated Pt bond pads
- Both packages successfully facilitated the test of SiC ICs in the simulated Venus environment
- Package insulation resistance excluded as primary DC leakage source
- Package insulation substantially degraded, possibly caused surface contaminations resulting from reactions of the impurities in alumina with Venus gases, and possible surface depositions from the simulated Venus environment



Surface encapsulation is suggested to improve electrical performance and reliability for possible long term Venus surface applications





Thank You Very Much for Your Attention!

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